REMARKS

Claims 1-19 are pending in this application, of which claims 11-17 have been withdrawn from consideration. Claims 18 and 19 are newly-added. Reconsideration of the rejections in view of these amendments and the following remarks is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment, which is captioned "Version with Markings to Show Changes Made."

Specification

The specification stands objected to for various informalities, which the Examiner deemed needed correction, as set forth in the outstanding Action.

Applicants respectfully submit that the amendments to the specification obviates the objection to the specification. Accordingly, withdrawal of the objection to the specification is respectfully solicited.

Drawings

The drawings stand objected to under 37 CFR 1.83(a).

The applicants respectfully request that the proposed drawing corrections submitted herewith be approved by the Examiner, and that the outstanding objection to the drawings be withdrawn.

Rejections under 35 U.S.C. §103

Claims 1, 2, 5 and 6 stand rejected under 35 U.S.C. 103(a) as being unpatentable over K. Kasai et al., *W/WNx/Poly-Si Gate Technology for Future High Speed Deep Submicron CMOS LSIs.*

Applicants respectfully traverse this rejection.

Claims 1, 2, 5 and 6 have a feature that the second polycrystalline silicon film has a thickness thinner than that of the first polycrystalline silicon film. In the present invention, the second polycrystalline silicon film, which has crystal grain boundaries discontinuous to the first polycrystalline silicon film, is formed between the first polycrystalline silicon film and the metal nitride film so as to prevent the dopant (boron) in the first polycrystalline silicon film from being absorbed by the metal nitride film. The diffusion of the dopant in the first polycrystalline silicon film toward the metal nitride film is suppressed by the second polycrystalline silicon film.

If, however, the second polycrystalline silicon film is too thick, contact resistance between the first polycrystalline silicon film and the metal nitride film is increased. There is a special concern that AC characteristics may be adversely affected. Thus, the thickness of the second polycrystalline silicon film must be thinner than that of the first polycrystalline silicon film. It is preferable that the second polycrystalline silicon film is 2-20 nm/thick (see page 8, line 18 to page 9, line 10 of the specification of the present application).

Kasai et al discloses the gate electrode including two silicon films. In Kasai et al, however, the lower silicon film formed on the gate insulation film (the polycrystalline silicon film: corresponding to the first

polycrystalline silicon film of the present invention) has a thickness of 100 nm. The upper silicon film formed on the lower silicon film (the amorphous silicon film: corresponding to the second polycrystalline silicon film of the present invention) is also 100 nm thick. Thus, the thickness of the upper silicon film is not less than that of the lower silicon film. Kasai et al does not teach or suggest the particular relationship between the thickness of the lower silicon film and the thickness of the upper silicon film. Also, Kasai et al does not teach or suggest the absorption of the dopant in the silicon film by the metal nitride film.

Thus, claims 1, 2, 5 and 6 patentably distinguish over Kasai et al.

Therefore, the 35 USC §103(a) rejection should be withdrawn.

Claims 1-10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukamoto (U.S. Pub. No. 2001/0000629) in view of K. Kasai et al.

Applicant respectfully traverse this rejection.

As discussed above, claims 1, 2, 5 and 6 recite that the second polycrystalline silicon film has a thickness less than that of the first polycrystalline silicon film. Claims 3, 4, and 7-10, depending from claim 1 or 2, also recite the same feature.

In Tsukamoto, however, the lower silicon film formed on the gate insulation film (the polycrystalline silicon film 10: corresponding to the first polycrystalline silicon film of the present invention) is 70 nm thick. The upper silicon film formed on the lower silicon film (the polycrystalline silicon film 11: corresponding to the second polycrystalline silicon film of the present invention) is also 70 nm thick. Thus, the thickness of the upper silicon film is not less than that of the lower silicon film.

Tsukamoto does not teach or suggest the particular relationship between the thickness of the lower silicon film and the thickness of the upper silicon film. Also, Tsukamoto does not teach or suggest the absorption of the dopant in the silicon film by the metal nitride film. Thus, Tsukamoto does not remedy the deficiencies of Kasai et al.

Therefore, claims 1-10 patentably distinguish over Kasai et al and Tsukamoto.

Therefore, the 35 USC §103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims , as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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PATENT TRADEMARK OFFICE

Enclosures: Version with Markings to Show Changes Made
Request for Approval of Drawing Corrections w/Figs. marked in red ink

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VERSION WITH MARKINGS TO SHOW CHANGES MADE S.N. 09/749,590

IN THE TITLE:

The title of the invention has been amended as follows:

SEMICONDUCTOR DEVICE ~~AND METHOD FOR FABRICATING THE SAME~~ HAVING GATE ELECTRODES WITH POLYMETAL STRUCTURE OF POLYCRYSTALLINE SILICON FILMS AND METAL FILMS

IN THE SPECIFICATION:

The paragraph beginning at page 23, line 20 has been amended as follows:

Next, the amorphous silicon film 18 is formed in a 10 nm-thick on the polycrystalline silicon film 16 by, e.g., CVD method (FIG. 6D). At this time, a native oxide ~~films (not shown) are~~ film 17 is formed between the polycrystalline silicon film 16 and the amorphous silicon film 18.

The paragraph beginning at page 29, line 5 has been amended as follows:

Next, a 10 nm-thick amorphous silicon film 18 is formed on the polycrystalline silicon film 40 by, e.g., CVD method (FIG. 11A). At this time, a native oxide ~~films (not shown) are~~ film is present between the polycrystalline silicon film 40 and the amorphous silicon film 18.

IN THE CLAIMS:

Claims 18 and 19 have been added.

Claims 1 and 2 have been amended as follows:

1. (Amended) A semiconductor device comprising:

a pair of impurity diffused regions formed in a silicon substrate, spaced from each other; and

a gate electrode formed above the silicon substrate between the pair of impurity diffused regions ~~intervening~~ with a gate insulation film interposed therebetween, the gate electrode being formed of a first polycrystalline silicon film formed on the gate insulation film, a second polycrystalline silicon film formed on the first polycrystalline silicon film having a thickness thinner than that of the first polycrystalline silicon film and having crystal grain boundaries which are discontinuous to the first polycrystalline silicon film, and a metal nitride film formed on the second polycrystalline silicon film.

2. (Amended) A semiconductor device comprising:

a pair of impurity diffused regions formed in a silicon substrate, spaced from each other; and

a gate electrode formed above the silicon substrate between the pair of impurity diffused regions ~~intervening~~ with a gate insulation film interposed therebetween, the gate electrode being formed of a first polycrystalline silicon film formed on the gate insulation film, a second polycrystalline silicon film formed on the first polycrystalline silicon film having a thickness thinner than that of the first polycrystalline silicon film

and having crystal grain boundaries which are discontinuous to the first polycrystalline silicon film, a metal nitride film formed on the second polycrystalline silicon film, and a metal film form on the metal nitride film.